

MILITARY DATA SHEET

Original Creation Date: 06/08/95
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Last Major Revision Date: 06/08/95

DUAL OPERATIONAL AMPLIFIER

MNLM1558-X REV 0B0

General Description

The LM1558 is a general purpose dual operational amplifier. The two amplifiers share a common bias network and power supply leads. Otherwise, their operation is completely independent.

Industry Part Number

NS Part Numbers

LM1558

LM1558H/883 LM1558J/883

Prime Die

LM1558

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp Description Temp ($^{\circ}$ C)

1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

- No frequency compensation required
- Short-circuit protection
- Wide common-mode and differential voltage ranges
- Low-power consumption
- 8-lead can and 8-lead mini DIP
- No latch up when input common mode range is exceeded

(Absolute Maximum Ratings)

Supply Voltage	<u>+</u> 22V			
Power Dissipation METAL CAN CERDIP	500mW TBD			
Differential Input Voltage	<u>+</u> 30V			
Input Voltage (Note 2)				
Output Short-Circuit Duration	<u>+</u> 15V			
	Continuous			
Operating Temperature Range	-55 C to +125 C			
Maximum Junction Temperature	150 C			
Storage Temperature Range	-65 C to +150 C			
Lead Temperature (Soldering 10 seconds)	260 C			
Thermal Resistance ThetaJA				
METAL CAN (Still Air) (500LF/Min Air flow)	TBD TBD			
CERDIP (Still Air) (500LF/Min Air flow)	TBD TBD			
ThetaJC METAL CAN CERDIP	TBD TBD			
ESD Tolerance (Note 3)				
	300V			

- Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

 Note 2: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

 Note 3: Human body model, 1.5K Ohms in series with 100pF.

Electrical Characteristics

DC PARAMETERS:

(The following conditions apply to all the following parameters, unless otherwise specified.) DC: Vcc = ± 15 V, Vcm = 0V, Rs = 10K Ohms

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN- NAME	MIN	MAX	UNIT	SUB- GROUPS
Vio	Input Offset Voltage	Vcm = -12V			-5	5	mV	1
	Voltage				-6	6	mV	2, 3
		Vcm = +12V			-5	5	mV	1
					-6	6	mV	2, 3
		Vcm = 0			-5	5	mV	1
					-6	6	mV	2, 3
		Vcc = 0, Rs = 50			-5	5	mV	1
					-6	6	mV	2, 3
		$Vcc = \pm 5V, Vcm = 0$			-5	5	mV	1
		$Vcc = \pm 5V, Vcm = 0$			-6	6	mV	2, 3
Iio	Input Offset Current	Vcm = -12V			-200	200	nA	1
					-500	500	nA	2, 3
		Vcm = +12V			-200	200	nA	1
					-500	500	nA	2, 3
		Vcm = 0			-200	200	nA	1
					-500	500	nA	2, 3
		$Vcc = \pm 5V, Vcm = 0$			-200	200	nA	1
		$Vcc = \pm 5V$, $Vcm = 0$			-500	500	nA	2, 3
Iib	Input Bias Current	Vcm = -12V				500	nA	1
	Gullens					1500	nA	2, 3
		Vcm = +12V				500	nA	1
						1500	nA	2, 3
		Vcm = 0				500	nA	1
						1500	nA	2, 3
		$Vcc = \pm 5V, Vcm = 0$				500	nA	1
		$Vcc = \pm 5V, Vcm = 0$				1500	nA	2, 3
PSRR	Power Supply Rejection Ratio	±5V, ≤ Vcc ≤15V			77		dB	1, 2,
CMRR	Common Mode Rejection Ratio	-12V ≤ Vcm ≤ 12V			70		dB	1, 2,

Electrical Characteristics

DC PARAMETERS:(Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.) DC: Vcc = ± 15 V, Vcm = 0V, Rs = 10K Ohms

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN- NAME	MIN	MAX	UNIT	SUB- GROUPS
Icc	Power Supply Current	Rs = 50 (Both Amplifiers Measured Together)				5	mA	1, 2
		logether,				7	mA	3
+Ios	Short Circuit Current	Rs = 50, Vout = 0V			-45	-14	mA	1
	Carrene				-45	-9	mA	2
					-50	-9	mA	3
-Ios	Short Circuit Current	Rs = 50, Vout = 0V			14	45	mA	1
	Gullens				9	45	mA	2
					9	50	mA	3
Vin	Input Voltage Range		1		-12	12	V	1, 2,
RIN	Input Resistance	(RIN = 5KT/qIib)	2		0.3		M Ohms	1
Vop+	Output Voltage Swing	Rs = 50, RL = 10K Ohms, Vcc = \pm 20V			16		V	4, 5, 6
		Rs = 50, RL = 2K Ohms, Vcc = \pm 20V			15		V	4, 5, 6
		Rs = 50, RL = 10K Ohms			12		V	4, 5, 6
		Rs = 50, RL = 2K Ohms			10		V	4, 5, 6
Vop-	Output Voltage Swing	Rs = 50, RL = 10K Ohms, Vcc = \pm 20V				-16	V	4, 5, 6
		Rs = 50, RL = 2K Ohms, Vcc = \pm 20V				-15	V	4, 5, 6
		Rs = 50, RL = 10K Ohms				-12	V	4, 5, 6
		Rs = 50, RL = 2K Ohms				-10	V	4, 5, 6
Avs+	Large Signal Voltage Gain	Rs = 50, RL = 2K, Vo = 10V			50		V/mV	4
	voitage Gain				25		V/mV	5, 6
Avs-	Large Signal Voltage Gain	Rs = 50, RL = 2K, Vo = -10V			50		V/mV	4
	voicage Gain				25		V/mV	5, 6

Electrical Characteristics

AC PARAMETERS:

(The following conditions apply to all the following parameters, unless otherwise specified.) AC: $Vcc = \pm 15V$, Vcm = 0

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN- NAME	MIN	MAX	UNIT	SUB- GROUPS
Sr+	Slew Rate	Vin = -5 to 5V			0.2		V/uS	9
		Vin = 5 to -5V, RL = 2K, CL = 100pF	2		0.2		V/uS	9
Sr-	Slew Rate	Vin = -5 to 5V			0.2		V/uS	9
		Vin = 5 to -5V, RL = 2K, CL = 100pF	2		0.2		V/uS	9
Gbw	Gain Bandwidth	Vin = 50mVrms, F = 20KHz, Rs = 50, RL = 2K			250		KHz	9
tr	Rise Time	RL = 2K Ohms, CL = 100pF	2			1	uS	9
os	Overshoot	RL = 2K Ohms, CL = 100pF	2			30	%	9

DC PARAMETERS: DRIFT VALUES

(The following conditions apply to all the following parameters, unless otherwise specified.) DC: $Vcc = \pm 15V$, Vcm = 0V, Rs = 10K Ohms. "Deltas not required on B-Level product. Deltas required for S-Level product ONLY as specified on Internal Processing Instructions (IPI)."

Vio	Input Offset Voltage	Vcm = 0		-1	1	mV	1
Iio	Input Offset Current	Vcm = 0		-20	20	nA	1

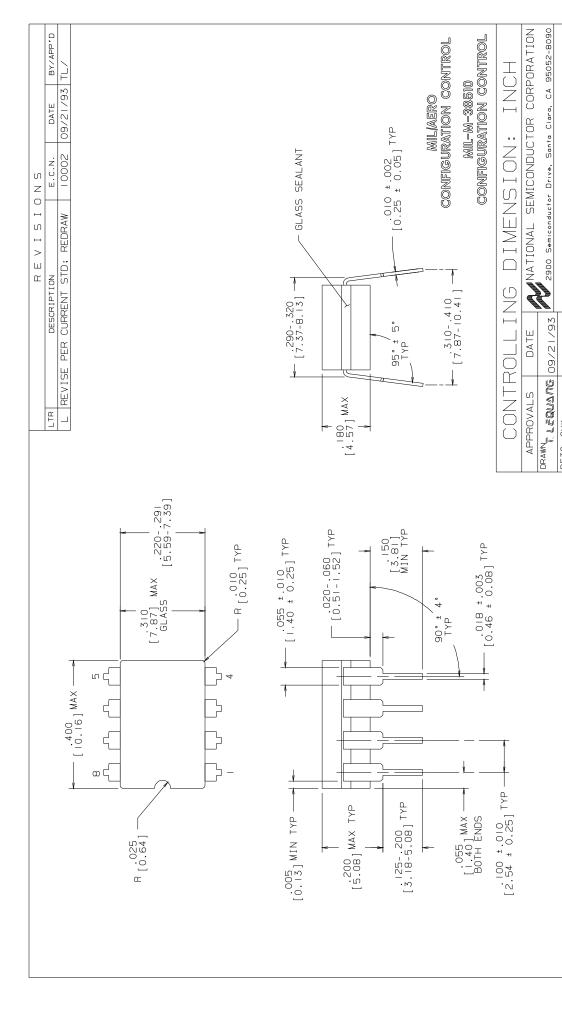
Guaranteed by the CMRR test.

Note 1: Note 2: Guaranteed parameter not tested.

Graphics and Diagrams

GRAPHICS#	DESCRIPTION
H08CRE	(blank)
J08ARL	CERDIP (J), 8 LEAD (P/P DWG)

See attached graphics following this page.



RE/

MKT-J08A

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PROJECTION

1. LEAD FINISH TO BE 200 MICROINCHES / 5.08 MICROMETERS MINIMUM SOLDER MEASURED AT THE CREST OF THE MAJOR FLATS. 2. JEDEC REGISTRATION MO-036, VARIATION AA, DATED 04/1981.

NOTES: UNLESS OTHERWISE SPECIFIED

DFTG. CHK. ENGR. CHK. APPROVAL CERDIP (, 8 LEAD

DO NOT SCALE DRAWING SHEET